WHAT IS CLAIMED IS:

1. A method for producing an electronic signal, comprising:

multiplying together a first phasor associated with the electronic signal with a delta phasor associated with a cyclic rate of the electronic signal to produce a second phasor, the first phasor having a first real portion and a first imaginary portion, the second phasor having a second real portion and a second imaginary portion;

adding the first imaginary portion to the first real portion to produce a first sum;

scaling the first sum according to a first scaling factor to produce an imaginary correction factor;

adding the imaginary correction factor to the second imaginary portion of the second phasor to correct for a magnitude error of the second phasor; and

updating the electronic signal based on the corrected second phasor.

2. The method of claim 1, further comprising:

subtracting the first imaginary portion from the first real portion to produce a first difference;

scaling the first difference according to the first scaling factor to produce a real correction factor; and

adding the real correction factor to the second real portion of the second phasor to further correct for the magnitude error of the second phasor.

3. The method of claim 1, wherein the first scaling factor is based on a bit-precision of N bits, where N is a non-zero integer.

4. The method of claim 3, wherein the first correction factor is further based on a second correction factor, the second correction factor being based on a first term of a Taylor series relating to a square-root.

5. The method of claim 4, wherein the second scaling factor is based on the formula:

$$\alpha = \left(\frac{1.0 - \left(\cos^2(\omega) + \sin^2(\omega)\right)}{2} \right)$$

where α is the second scaling factor and ω is the frequency of the complex sinusoid.

6. The method of claim 5, wherein the second correction factor is determined according to the formula $\alpha \approx 2^{-P}$, where **P** is a non-zero integer.

7. The method of claim 6, wherein the first scaling factor is equal to $2^{-(P+N)}$.

8. The method of claim 7, wherein the step of scaling is performed using a shift operation.

9. The method of claim 1, wherein the step of scaling is performed using a shift operation.

10. The method of claim 1, further comprising updating the electronic signal based on a third phasor produced a high-accuracy technique.

11. The method of claim 1, wherein the electronic signal is an electronic analog signal having sinusoidal form.

12. The method of claim 1, further comprising producing a communication signal based on the updated electronic signal.

13. The method of claim 1, further comprising receiving a communication signal using the updated electronic signal.

14. The method of claim 2, wherein the steps of scaling are performed using a shift operation of N+P bits, where N is a target bit-precision and P is a non-zero integer such that

$$2^{-P} \approx \left(\frac{1.0 - \left(\cos^2(\omega) + \sin^2(\omega)\right)}{2} \right)$$

where ω is the frequency of the complex sinusoid.

15. An apparatus for producing an electronic signal, comprising:

a multiplier that multiplies a first phasor associated with the electronic signal and a delta phasor associated with a cyclic rate of the electronic signal to produce a second phasor, the first phasor having a first real portion and a first imaginary portion, the second phasor having a second real portion and a second imaginary portion;

an arithmetic device that adds the first imaginary portion to the first real portion to produce a first sum;

a scaling device that scales the first sum according to a first scaling factor to produce an imaginary correction factor;

an adding device that adds the imaginary correction factor to the second imaginary portion of the second phasor to correct for a magnitude error of the second phasor; and

an interface that updates the electronic signal based on the corrected second phasor.

16. The method of claim 15, wherein the electronic signal is an electronic analog signal having sinusoidal form.

17. The method of claim 15, wherein the electronic signal is a communication signal having embedded information.

18. The apparatus of claim 15, wherein the arithmetic device further subtracts the first imaginary portion from the first real portion to produce a first difference, the scaling device further scales the first difference according to the first scaling factor to produce a real correction factor; and the adding device further adds the real correction factor to the second real portion of the second phasor to further correct for the magnitude error of the second phasor.

19. The apparatus of claim 15, wherein the first scaling factor is based on a bit-precision of N bits, where N is a non-zero integer.

20. The apparatus of claim 15, wherein the first correction factor is further based on a second correction factor, the second correction factor being based on a first term of a Taylor series.

21. The apparatus of claim 16, wherein the second scaling factor is based on the formula:

$$\alpha = \left(\frac{1.0 - \left(\cos^2(\omega) + \sin^2(\omega)\right)}{2} \right)$$

where α is the second scaling factor and ω is the frequency of the complex sinusoid.

22. The apparatus of claim 21, wherein the second correction factor is determined according to the formula $\alpha = 2^{-P}$, where P is a non-zero integer.

23. The apparatus of claim 22, wherein the scaling device scales the first sum device using a shift operation.

24. The apparatus of claim 15, wherein the scaling device scales the first sum device using a shift operation.

25. The apparatus of claim 15, wherein the apparatus further updates the electronic signal based on a third phasor, the third phasor being produced a high-accuracy technique.

26. A machine-readable medium including instructions for producing an electronic signal, the instructions being arranged to cause a machine to perform the steps of:

multiplying a first phasor associated with the electronic signal and a delta phasor associated with a cyclic rate of the electronic signal to produce a second phasor, the first phasor having a first real portion and a first imaginary portion, the second phasor having a second real portion and a second imaginary portion;

adding the first imaginary portion to the first real portion to produce a first sum;

scaling the first sum according to a first scaling factor to produce an imaginary correction factor;

adding the imaginary correction factor to the second imaginary portion of the second phasor to correct for a magnitude error of the second phasor; and

updating the electronic signal based on the corrected second complex sinusoid phasor.

27. The machine-readable medium of claim 26, further comprising instructions being arranged to cause a machine to perform the steps of:

subtracting the first imaginary portion from the first real portion to produce a first difference;

scaling the first difference according to the first scaling factor to produce a real correction factor; and

adding the real correction factor to the second real portion of the second phasor to further correct for the magnitude error of the second phasor.

28. The machine-readable medium of claim 27, wherein the steps of scaling are performed using a shift operation of N+P bits, where N is a target bit-precision and P is a non-zero integer such that

$$2^{-P} \approx \left(\frac{1.0 - \left(\cos^2(\omega) + \sin^2(\omega)\right)}{2} \right)$$

where ω is the frequency of the complex sinusoid.

29. An apparatus for producing an electronic signal, comprising:

a multiplying means for multiplying a first phasor associated with the electronic signal and a delta phasor associated with a cyclic rate of the electronic signal to produce a second phasor, the first phasor having a first real portion and a first imaginary portion, the second phasor having a second real portion and a second imaginary portion;

an arithmetic means for adding the first imaginary portion to the first real portion to produce a first sum;

a scaling means for scaling the first sum according to a first scaling factor to produce an imaginary correction factor;

an adding means for adding the imaginary correction factor to the second imaginary portion of the second phasor to correct for a magnitude error of the second phasor;

an interface that updates the electronic signal based on the corrected second phasor.

30. The apparatus of claim 29, wherein the arithmetic means further subtracts the first imaginary portion from the first real portion to produce a first difference, the scaling means further scales the first difference according to the first scaling factor to produce a real correction factor; and the adding means further adds the real correction factor to the second real portion of the second phasor to further correct for the magnitude error of the second phasor.

31. The apparatus of claim 29, wherein the scaling means performs its scaling without using a multiply operation.

32. The apparatus of claim 29, wherein the scaling means performs its scaling using one or more shift operations.

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33. The apparatus of claim 29, further comprising a communication-based device that produces a communication signal using the updated electronic signal.

34. The apparatus of claim 29, further comprising a communication-based device that receives a communication signal using the updated electronic signal.